CLAIMS

Please amend claim 1, cancel claim 8, all without prejudice as follows.

1 (currently amended): A semiconductor device structure, comprising:

at least first and second field effect transistors disposed on a substrate;

said first field effect transistor including a first spacer having a first width;

said second field effect transistor including a second spacer having a second width;

wherein said first spacer and second spacer ~~includes~~ include a first compressive stress material, and said structure further comprises a tensile stress material disposed on said at least first and second field effect transistors.

2 (original): The structure as claimed in claim 1, wherein said first field effect transistor is an nFET and said second field effect transistor is a pFET.

3 (original): The structure as claimed in claim 1, wherein said first width is less than said second width.

4 (original): The structure as claimed in claim 1, wherein said structure is an inverter.

5 (original): The structure as claimed in claim 1, wherein said structure includes a width transition region located approximately in a middle region between said transistors.

6 (original): The structure as claimed in claim 1, wherein said first spacer includes an I-shaped part and said second spacer includes an L-shaped part.

7 (original): The structure as claimed in claim 1, wherein said second spacer includes an L-shaped part and said first compressive stress material.

8 (cancelled)

9 (original): The structure as claimed in claim 1, wherein said first width is a substantially uniform width in a range of about 10 nm to about 30 nm, and said second width has a maximum width in a range of about 50 nm to about 120 nm.

10 (original): The structure as claimed in claim 1, wherein said first compressive stress material has a substantially uniform stress in a range of about -3E9 dynes/cm^2 to about -3E11 dynes/cm^2.

11 (original): The structure claimed in claim 1, wherein said tensile stress material has a substantially uniform film thickness in a range of about 20 nm to about 100 nm and a substantially uniform stress in a range of approximately 4E9 dynes/cm^2 to approximately 4E11 dynes/cm^2.

12 (original): The structure as claimed in claim 1, wherein said second spacer includes a second compressive stress material having a stress in a range of approximately -2E9 dynes/cm^2 to approximately 2E9 dynes/cm^2.

13 (original): The structure as claimed in claim 1, wherein said first compressive stress material is a dielectric.

14 (original): The structure as claimed in claim 1, wherein said first compressive stress material is silicon nitride.

15 (original): The structure as claimed in claim 1, wherein said tensile stress material is SiN.

16 (original): The structure as claimed in claim 1, wherein said first width is about 50 nm, and said second width has a maximum width of about 90 nm.

17 (original): The structure as claimed in claim 1, wherein said tensile stress material is a layer having a substantially uniform thickness in a range of about 20 nm to about 100 nm.

18 (withdrawn): A method for fabricating a semiconductor device structure, comprising: -providing a semiconductor substrate;

forming gate stacks on the substrate, extension spacers on the gate stacks, extension implants adjacent to the extension spacers, and an isolation region between at least two extension implants;

disposing a first compressive stress dielectric material onto the gate stacks, extension spacers, and extension implants;

disposing a second dielectric material with a low stress onto the first compressive stress dielectric material;

masking a first portion of the second dielectric material over one gate stack;

removing a second portion of the second dielectric material over another gate stack;

etching the first portion to form intermediate low stress spacers proximate to the one gate stack;

etching the first dielectric material to form narrow compressive spacers proximate to the another gate stack and wide compressive spacers proximate to the one gate stack;

forming source and drain implants and silicides thereon;

disposing a tensile stress dielectric material over all the spacers.

19 (withdrawn): The method as claimed in claim 18, wherein said step of disposing a first compressive stress dielectric material includes PECVD depositing silicon nitride.

20 (withdrawn): The method as claimed in claim 18, wherein said step of disposing a tensile stress dielectric material includes CVD depositing a SiN layer.

21 (previously presented): The structure as claimed in claim 1, wherein said substrate is a silicon substrate.

22 (previously presented): The structure as claimed in claim 1, wherein said substrate comprises GaAs.